Remarks

The Examiner has objected to the drawings for failing to comply with 37 C.F.R. §1.84(p)(5) because they include reference sign 16 in figure 3A and reference sign 36 in figure 3B. The Examiner has rejected claims 1-41 under 35 U.S.C. §103(a) as being unpatentable over Lam, United States Patent Number 6,281,046 in view of admitted prior art described on pages 2-4 of the specification.

Objection to the Drawings

The Examiner has objected to the drawings for failing to comply with 37 C.F.R. §1.84(p)(5) because they include reference sign 16 in figure 3A and reference sign 36 in figure 3B. The Applicant has amended the specification to add description of the conductive attachment elements 16 depicted figure 3A and the conductive attachment elements 36 depicted in figure 3B. Accordingly, the Applicant believes the basis for the drawing objection has been overcome and requests that the Examiner withdraw the drawing objection.

Rejection Under 35 U.S.C. §103(a)

The Examiner has rejected claims 1-41 under 35 U.S.C. §103(a) as being unpatentable over Lam, in view of admitted prior art described on pages 2-4 of the specification. The Applicant has

carefully reviewed Lam and the description of the prior art in the Background of the Invention section of the present application. The Applicant has also amended claims 1-13, 18-30, 36 and 41 to more clearly describe the present invention.

The Examiner states that Lam teaches electrically and mechanically coupling a semiconductor wafer 21 having a plurality of integrated circuit chips 25 to an interposer 31 to form a wafer-interposer assembly 39, testing the integrated circuit chips 25 of the semiconductor wafer 21 and dicing the wafer-interposer assembly 39 into a plurality of chip assemblies. The Examiner also states that Lam does not expressly teach selecting at least two of the chip assemblies for inclusion in the matched set based upon the testing. The Examiner further states that the prior art as described in the Background of the Invention section of the present application teaches that each chip has been tested prior to inclusion in the matched set.

The applicant has amended claim 1 to specifically recite that at least two of the integrated circuit chips are simultaneously tested at the wafer-interposer assembly level and that the at least two simultaneously tested integrated circuit chips are selected for inclusion in the matched set based upon the simultaneous testing. This simultaneous testing is particularly advantageous when the integrated circuit chips are to be included in a chip collections as this simultaneous testing not only provides efficiency to the

testing process, but also, allows for a determination of which integrated circuit chips match up best with one another. This allows for optimization of the overall performance of specific matched sets as well as the overall performance of all the matched sets made from integrated circuit chips from a single wafer.

As the Examiner states, Lam teaches attaching a prefabricated interposer substrate to a wafer to form a wafer-interposer assembly that is diced into individual BGA chip packages. Also, as the Examiner states, Lam does not teach selecting at least two of the chip assemblies for inclusion in the matched set based upon the testing. Accordingly, Lam does not teach, suggest or disclose the simultaneous testing of at least two of the integrated circuit chips at the wafer-interposer assembly level and that the at least two simultaneously tested integrated circuit chips are selected for inclusion in the matched set based upon the simultaneous testing as now recited in claim 1.

The Examiner states that the prior art as described in the Background of the Invention section of the present application teaches that each chip has been tested prior to inclusion in the matched set. The Background of the Invention specifically states that:

> Typically, each of the identical components has been extensively tested individually prior to inclusion in this type of system. The individual characterization tests for a filter, for instance, might measure insertion loss and phase shift as a function of frequency, input power and temperature. These multi-dimensional arrays of

> data are then compared to each other to identify individual components that perform within acceptable limits relative to each other. Components that are found to exhibit similar behavior under the various input stimuli will constitute a matched set of identical devices. Conversely, components that are found to exhibit dissimilar behavior under the various input stimuli, for example, the gain of one component having a negative slope over temperature while the gain of another component having a positive slope over temperature, will constitute a mismatch of components that will not be placed in a chip collection.

The Background of the Invention goes on to state that:

> It has been found, however, [that] certain mismatches are not identified when the components are tested individually. In fact, certain mismatches are not identified until the entire chip collection is assembled and the components are tested together for the first time. As such, some chip collections must be disassembled so that the valuable components may be, for example, packaged as individual components, while other chip collections are simple discarded.

The present invention, as defined by claim 1, is specifically designed to overcome the prior art problem associated with assembling various components together into a chip collection when the testing of the component parts has occurred only at the individual chip level not at the group level prior to assembling the chip collection. Even though components may exhibit similar characteristics when tested individually, this does not assure compatibility when the component are used together in a chip collection. Quite unlike the prior art as described in the Background of the Invention section of the present application, the present invention as defined by claims 1 provides for the

simultaneous testing of at least two of the integrated circuit chips at the wafer-interposer assembly level and for the selection of the at least two simultaneously tested integrated circuit chips for inclusion in the matched set based upon the simultaneous testing.

For at least the foregoing reasons, the Applicant believes that claim 1 is patentably distinguishable and nonobvious over Lam, either alone or in combination with the prior art as described in the Background of the Invention section of the present application. Accordingly, the Applicant requests that the Examiner withdraw the outstanding rejection and allow claim 1. In addition, as claims 2-17 depend from claim 1 and add further limitations, the Applicant requests that the Examiner withdraw the outstanding rejections and allow claims 2-17.

The Applicant has amended claim 18 to specifically recite that pairs of integrated circuit chips of a wafer are simultaneously tested at the wafer-interposer assembly level then sorted based upon the simultaneous testing of the pairs of the integrated circuit chips prior to being electrically coupled onto a substrate creating the matched set. As stated above, neither Lam nor the prior art as described in the Background of the Invention section of the present application either alone or in combination, teach, suggest or disclose such a testing and selection process for assembling a matched set as defined by claim 18.

For at least the foregoing reasons, the Applicant believes that claim 18 is patentably distinguishable and nonobvious over Lam, either alone or in combination with the prior art as described in the Background of the Invention section of the present application. Accordingly, the Applicant requests that the Examiner withdraw the outstanding rejection and allow claim 18. In addition, as claims 19-34 depend from claim 18 and add further limitations, the Applicant requests that the Examiner withdraw the outstanding rejections and allow claims 19-34. Also, as claim 35 is based upon claim 18, the Applicant requests that the Examiner withdraw the outstanding rejection and allow claim 35.

The applicant has amended claim 36 to specifically recited that first and second chip assemblies diced from a wafer-interposer assembly that respectively include first and second integrated circuit chips from a wafer that have been previously simultaneously tested as part of the wafer-interposer assembly are electrically coupled to a substrate to form a matched set.

As stated above, neither Lam nor the prior art as described in the Background of the Invention section of the present application either alone or in combination, teach, suggest or disclose such testing and selection of integrated circuit chips for assembly into a matched set as defined by claim 36.

For at least the foregoing reasons, the Applicant believes that claim 36 is patentably distinguishable and nonobvious over

Lam, either alone or in combination with the prior art as described in the Background of the Invention section of the present application. Accordingly, the Applicant requests that the Examiner withdraw the outstanding rejection and allow claim 36. In addition, as claims 37-41 depend from claim 36 and add further limitations, the Applicant requests that the Examiner withdraw the outstanding rejections and allow claims 37-41.

Conclusion

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the outstanding objections and rejections and allow claims 1-41 presented for reconsideration herein. Accordingly, a favorable action in the form of an early notice of allowance is respectfully requested. The Examiner is requested to call the undersigned for any reason that would advance the instant application to issue.

Fee Statement

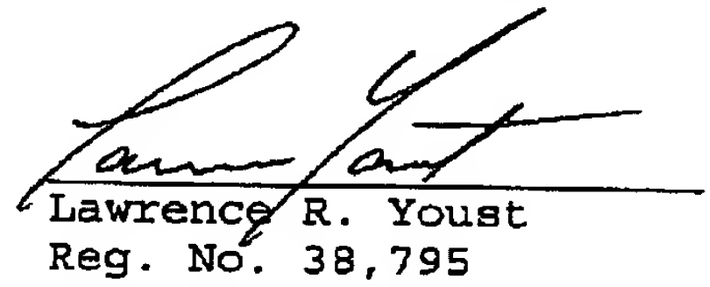
Form PTO-2038 is submitted herewith authorizing the Commissioner to charge $460.00 to the indicated account for an Extension for Response within Third Month under 37 C.F.R. §1.17(a)(3). Accordingly, Applicant believes no additional fees are due for the filing of this Response. If any additional fees

are due, or any overpayments have been made, however, please charge, or credit, our Deposit Account No. 03-1130.

The Examiner is requested to call the undersigned for any reason that would advance the instant application to issue.

Dated this 17th day of April, 2002.

Respectfully submitted:



Lawrence R. Youst
Reg. No. 38,795
Danamraj & Youst, P.C.
12900 Preston Road
Suite 1200, LB-15
Dallas, Texas 75230
(972)392-2696
(972)720-1139 (fax)

Marked Up Claims per 37 C.F.R. §1.121(c)(1)(ii)

The following is the replacement paragraph in marked up format for the paragraph beginning on page 14, line 21 and extending to page 15, line 13:

Referring next to figure 3A a cross sectional view of interposer 12 taken along line 3A-3A of figure 1 is depicted wherein conductive attachment elements 16 have been attached thereto. Interposer 12 includes a plurality of layers having routing lines and vias therein which serve as electrical conductors. One set of conductors, depicted as conductors 50, 52, 54 and 56, pass through interposer 12 and serve to electrically connect pads 26 of chips 24 to the contact pads 22 of interposer 12. These conductors are selected to have suitable conductivity and may be, for example, aluminum or copper. Interposer 12 also includes a set of testing conductors, depicted as conductor 58, that pass through interposer 12 connecting some of the contact pads 26 of chips 24 to a testing apparatus as will be explained in greater detail below. The testing conductors may provide direct electrical connection to the testing apparatus or may pass through a multiplexer or other intervening apparatus (not shown) incorporated into interposer 12.

The following is the replacement paragraph in marked up format for the paragraph on page 17, line 7-19:

For example, as best seen in figure 3B, interposer 32, which has conductive attachment elements 36 attached thereto, includes a plurality of layers having routing lines and vias therein which serve as electrical conductors. One set of conductors, depicted as conductors 60, 62, 64 and 66 pass through interposer 32 to electrically connect contact pads 42 on the upper surface of interposer 32 to contact pads 46 on chips 44 (see figure 2). Another set of conductors, depicted as conductors 68 and 70, are testing conductors that pass through interposer 32 and are used to connect certain pads 46 of chips 44 (see figure 2) to a testing apparatus, as will be explained in greater detail below. As such, the geometry of pads 42 on the upper surface of interposer 32 is different from that of pads 46 on chips 44.

Marked Up Claims per 37 C.F.R. §1.121(c)(1)(ii)

1. (Amended) A method for selecting components for a matched set comprising the steps of:

electrically and mechanically coupling a semiconductor wafer having a plurality of integrated circuit chips to an interposer to form a wafer-interposer assembly;

simultaneously testing at least two of the integrated circuit chips of the semiconductor wafer;

dicing the wafer-interposer assembly into a plurality of chip assemblies; and

selecting at least two of the chip assemblies corresponding to the at least two of the integrated circuit chips for inclusion in the matched set based upon the simultaneous testing.

2. (Amended) The method as recited in claim 1 wherein the step of simultaneously testing at least two of the integrated circuit chips further comprises simultaneously testing groups of the integrated circuit chips together to identify which groups of integrated circuit chips perform best together for inclusion in a selected number of high performance matched sets.

3. (Amended) The method as recited in claim 1 wherein the step of simultaneously testing at least two of the integrated circuit chips further comprises simultaneously testing groups of integrated circuit chips together to grade the groups of integrated circuit chips for performance such that the overall performance of matched sets assembled from the chip assemblies is maximized.

4. (Amended) The method as recited in claim 1 wherein the step of simultaneously testing at least two of the integrated circuit chips further comprises simultaneously testing groups of the integrated circuit chips together to identify the compatibility of individual integrated circuit chips with one another.

5. (Amended) The method as recited in claim 1 wherein the step of simultaneously testing at least two of the integrated circuit chips further comprises simultaneously testing groups of the integrated circuit chips together to identify which individual integrated circuit chips are incompatible with one another.

6. (Amended) The method as recited in claim 1 wherein the step of simultaneously testing at least two of the integrated circuit chips further comprises simultaneously testing the at least two of the integrated circuit chips for performance over a range of temperatures.

7. (Amended) The method as recited in claim 1 wherein the step of simultaneously testing at least two of the integrated circuit chips further comprises simultaneously performing burn-in testing of the at least two of the integrated circuit chips.

8. (Amended) The method as recited in claim 1 wherein the step of simultaneously testing at least two of the integrated circuit chips further comprises simultaneously vibrating the at least two of the integrated circuit chips.

9. (Amended) The method as recited in claim 1 wherein the step of simultaneously testing at least two of the integrated circuit chips further comprises simultaneously testing the at least two of the integrated circuit chips for leakage currents.

10. (Amended) The method as recited in claim 1 wherein the step of simultaneously testing at least two of the integrated circuit chips further comprises simultaneously testing the at least two of the integrated circuit chips for offset voltages.

11. (Amended) The method as recited in claim 1 wherein the step of simultaneously testing at least two of the integrated circuit chips further comprises simultaneously testing the at least two of the integrated circuit chips for gain tracking.

12. (Amended) The method as recited in claim 1 wherein the step of simultaneously testing at least two of the integrated circuit chips further comprises simultaneously testing the at least two of the integrated circuit chips for bandwidth.

13. (Amended) The method as recited in claim 1 wherein the step of simultaneously testing at least two of the integrated circuit chips further comprises simultaneously testing the at least two of the integrated circuit chips for speed grades.

18. (Amended) A method for assembling a matched set comprising the steps of:

providing a semiconductor wafer having a plurality of integrated circuit chips;

electrically and mechanically coupling the wafer to an interposer to form a wafer-interposer assembly;

simultaneously testing pairs of the integrated circuit chips of the wafer;

dicing the wafer-interposer assembly into a plurality of chip assemblies;

sorting the chip assemblies based upon the simultaneous testing of the pairs of the integrated circuit chips; and

electrically coupling at least two of the chip assemblies corresponding to a sorted pair of the integrated circuit chip onto a substrate, thereby assembling the matched set.

19. (Amended) The method as recited in claim 18 wherein the step of simultaneously testing pairs of the integrated circuit chips further comprises simultaneously testing groups of the integrated circuit chips together to identify which groups of integrated circuit chips perform best together for inclusion in a selected number of high performance matched sets.

20. (Amended) The method as recited in claim 18 wherein the step of simultaneously testing pairs of the integrated circuit chips further comprises simultaneously testing groups of integrated circuit chips together to grade the groups of integrated circuit chips for performance such that the overall performance of matched sets assembled from the chip assemblies is maximized.

21. (Amended) The method as recited in claim 18 wherein the step of simultaneously testing pairs of the integrated circuit chips further comprises simultaneously testing groups of the integrated circuit chips together to identify the compatibility of individual integrated circuit chips with one another.

22. (Amended) The method as recited in claim 18 wherein the step of simultaneously testing pairs of the integrated circuit chips further comprises simultaneously testing groups of the integrated circuit chips together to identify which individual integrated circuit chips are incompatible with one another.

23. (Amended) The method as recited in claim 18 wherein the step of simultaneously testing pairs of the integrated circuit chips further comprises simultaneously testing the pairs of the integrated circuit chips for performance over a range of temperatures.

24. (Amended) The method as recited in claim 18 wherein the step of simultaneously testing pairs of the integrated circuit chips further comprises simultaneously performing burn-in testing of the pairs of the integrated circuit chips.

25. (Amended) The method as recited in claim 18 wherein the step of simultaneously testing pairs of the integrated circuit chips further comprises simultaneously vibrating the pairs of the integrated circuit chips.

26. (Amended) The method as recited in claim 18 wherein the step of simultaneously testing pairs of the integrated circuit chips further comprises simultaneously testing the pairs of the integrated circuit chips for leakage currents.

27. (Amended) The method as recited in claim 18 wherein the step of simultaneously testing pairs of the integrated circuit chips further comprises simultaneously testing the pairs of the integrated circuit chips for offset voltages.

28. (Amended) The method as recited in claim 18 wherein the step of simultaneously testing pairs of the integrated circuit chips further comprises simultaneously testing the pairs of the integrated circuit chips for gain tracking.

29. (Amended) The method as recited in claim 18 wherein the step of simultaneously testing pairs of the integrated circuit chips further comprises simultaneously testing the pairs of the integrated circuit chips for bandwidth.

30. (Amended) The method as recited in claim 18 wherein the step of simultaneously testing pairs of the integrated circuit chips further comprises simultaneously testing the pairs of the integrated circuit chips for speed grades.

36. (Amended) A matched set of integrated circuit chips [including at least two integrated circuit chips from wafer, the integrated circuit chips being tested together as part of a wafer-interposer assembly including the wafer and a wafer interposer, the matched set] comprising:

a first chip assembly diced from [the] a wafer-interposer assembly, the first chip assembly including a first integrated circuit chip from a wafer;

a second chip assembly diced from the wafer-interposer assembly, the second chip assembly including a second integrated circuit chip from the wafer, the first and second integrated circuit chips being previously simultaneously tested as part of the wafer-interposer assembly; and

a substrate on to which the first and second chip assemblies are electrically coupled.

41. (Amended) The matched set as recited in claim 36 further comprising a third chip assembly diced from the wafer-interposer assembly, the third chip assembly including a third integrated circuit chip from the wafer, the first, second and third integrated circuit chips being previously simultaneously tested as part of the wafer-interposer assembly, the third chip assembly electrically coupled to the substrate.